ABSTRACT

A dynamic PLA (DPLA) that combines registers and dynamic PLA to make the array "reprogrammable" after the array is built is disclosed. The DPLA comprises at least one logic plane; and at least one reprogrammable evaluate module within the at least one logic plane. The at least one reprogrammable evaluate module includes a first program input, a second program input, a storage element coupled to the first and second program inputs, and an input pass transistor whose gate is coupled to the output of the storage element and whose source and drain are coupled to a control input and the gate of an evaluate transistor. In such a DPLA, the AND plane and OR plane are fully populated with reprogrammable evaluate modules such that every input signal can be programmed to affect every AND term output and every AND term signal can be programmed to affect every OR term output.